GAU2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Docket No.: 303.586US1
Filed: May 26, 1999
Examiner: Anh-Quan Tra

Serial No.: 09/320,421
Due Date: October 18, 2001
Group Art Unit: 2816

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response under 37 CFR 1.111 (11 Pages).
X Clean Version of Pending Claims (10 pgs.).
X Clean Version of Amended Specification Paragraph (1 pg.).
X Red-Line Drawing of Figure 2A (1 pg.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 10th day of October, 2001.

Amy Moriarty
Name

Amy Moriarty
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(GENERAL)

#12/C+ Drawing Changes

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10/23/01 A Smith

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on July 18, 2001. Please amend the above-identified patent application as follows.

IN THE DRAWINGS

The drawings were objected to under 37 CFR 1.83(a).

Enclosed is a copy of Figure 2A of the drawings showing the following proposed amendment to Figure 2A in red ink.

The transistors M3 and M5 are part of a single dual-gated MOSFET as cited on page 10, lines 16-18. A dashed box, labeled 298, enclosing M3 and M5 is used to represent a single dual-gated MOSFET. The transistors M4 and M6 are part of a single dual-gated MOSFET as cited on page 10, lines 16-18. A dashed box, labeled 299, enclosing M4 and M6 is used to represent a single dual-gated MOSFET. No new matter has been introduced by this inclusion of the labeled boxes.

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning at page 10, line 16 is amended as follows:

In an alternative embodiment, the pair of transistors, M3, M5, and M4, M6, in each inverter, B1 and B2, comprise a dual-gated metal oxide semiconductor field effect transistor (MOSFET), 298 and 299, respectively, in each inverter, B1 and B2. In this embodiment, each one of the pair of input transmission lines is coupled to a first gate of the dual-gated MOSFET in